T09290 T6226860

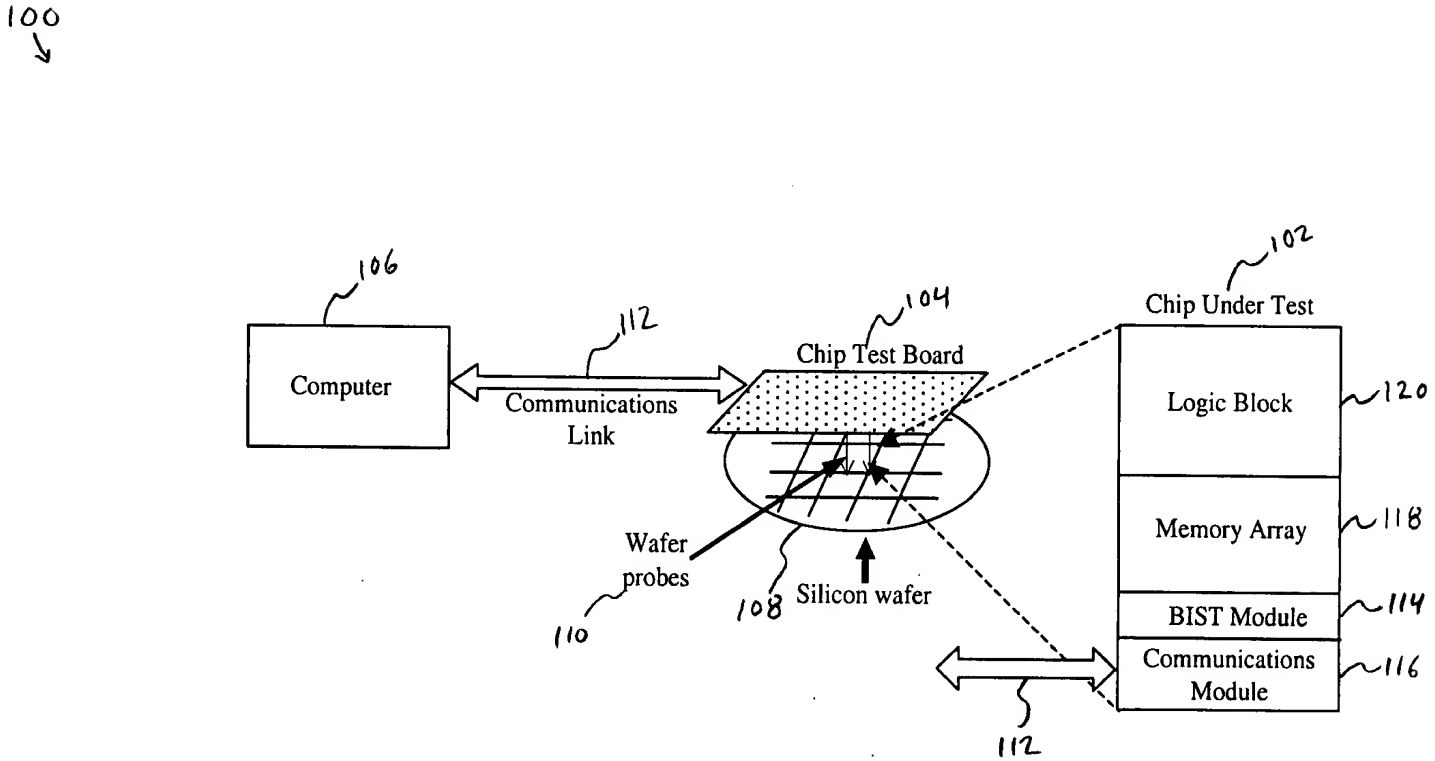


Fig. 1

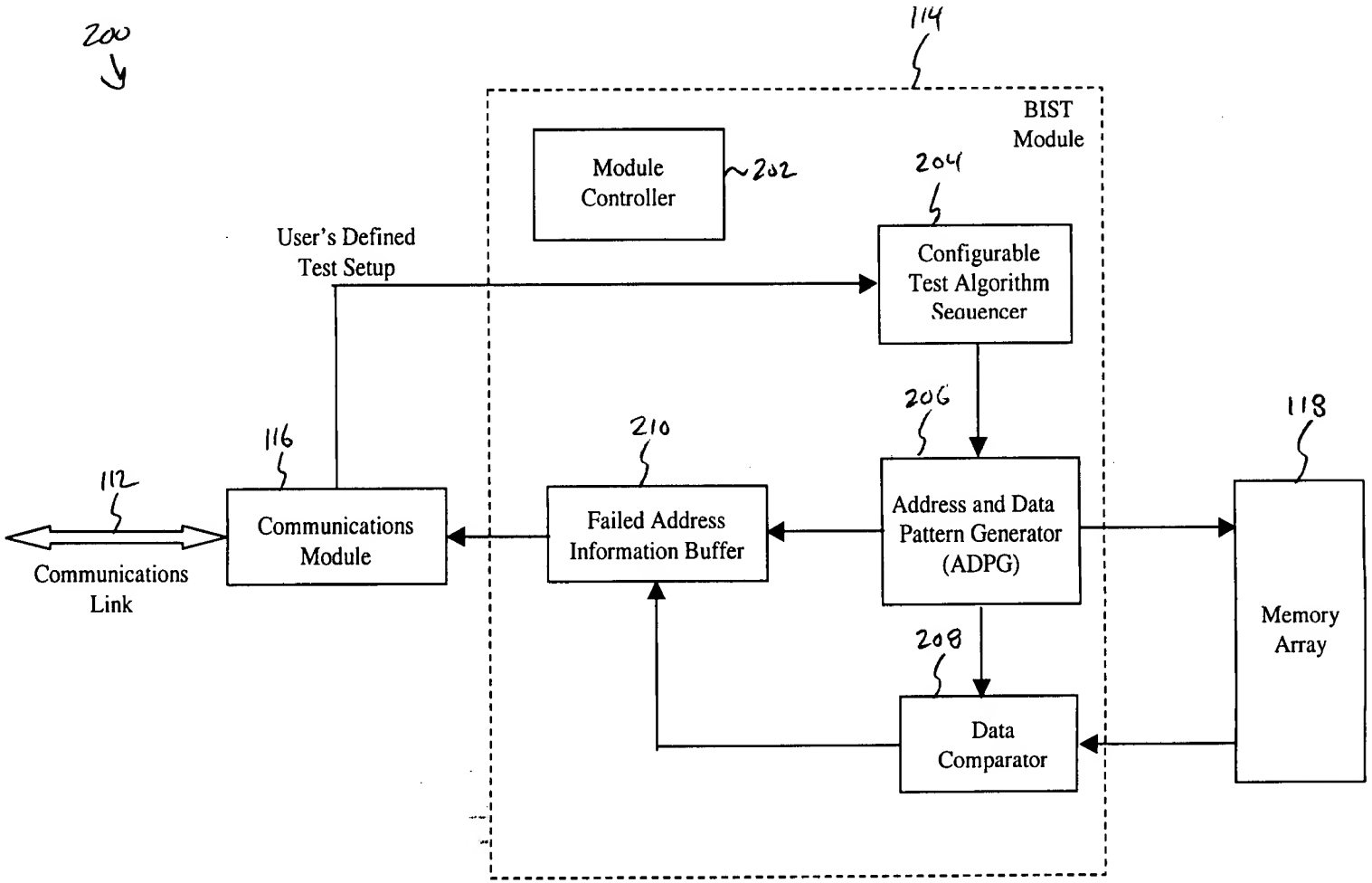

200
114
BIST Module
Module Controller
202
204
User's Defined Test Setup
Configurable Test Algorithm Sequencer
206
210
118
116
112
Communications Module
Failed Address Information Buffer
Address and Data Pattern Generator (ADPG)
Memory Array
Communications Link
208
Data Comparator

Fig. 2

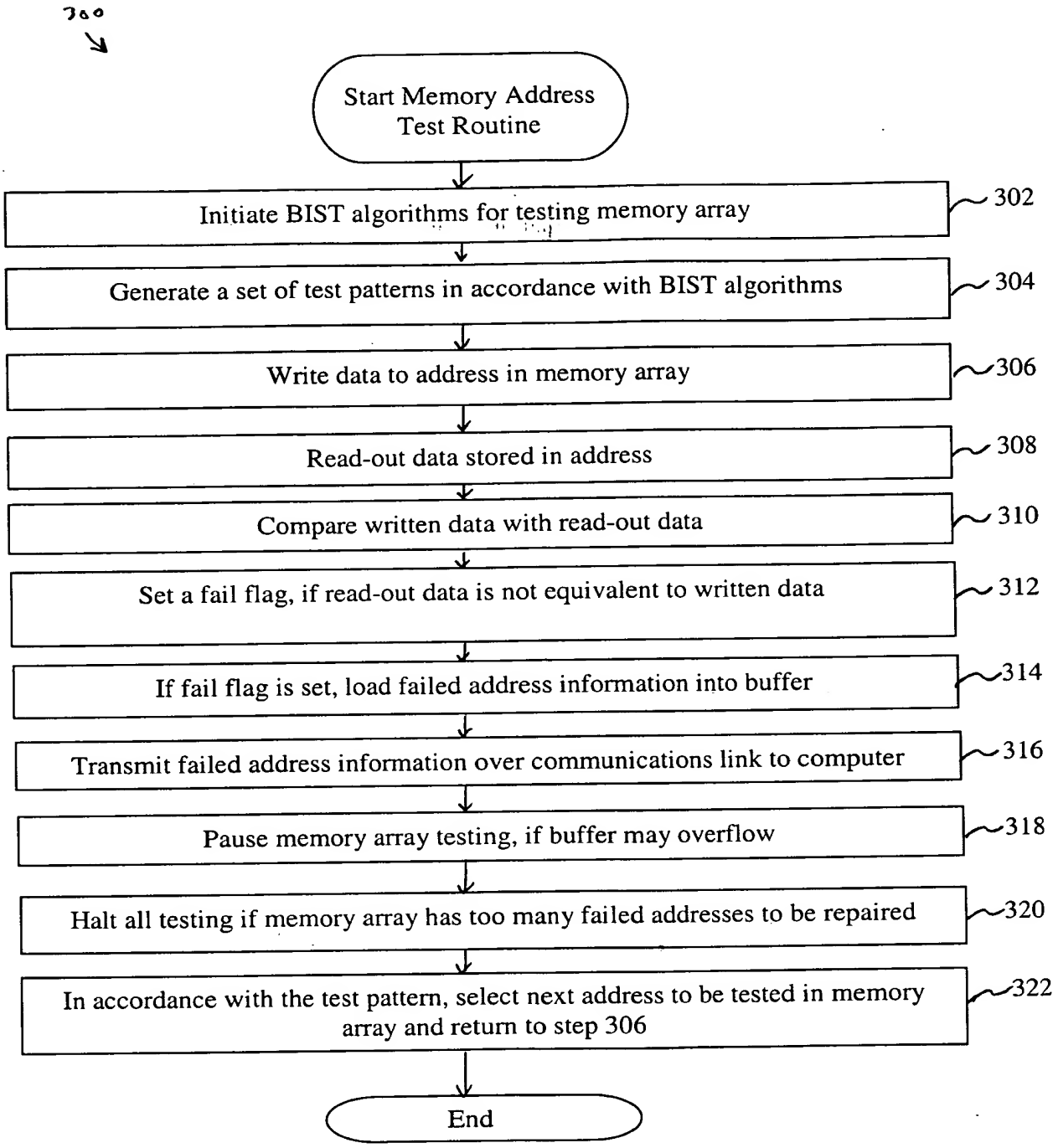
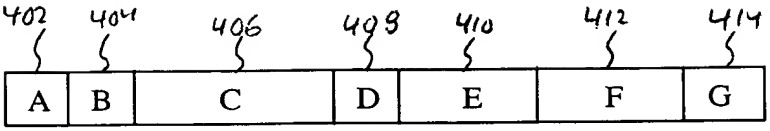

300
Start Memory Address Test Routine
Initiate BIST algorithms for testing memory array
302
Generate a set of test patterns in accordance with BIST algorithms
304
Write data to address in memory array
306
Read-out data stored in address
308
Compare written data with read-out data
310
Set a fail flag, if read-out data is not equivalent to written data
312
If fail flag is set, load failed address information into buffer
314
Transmit failed address information over communications link to computer
316
Pause memory array testing, if buffer may overflow
318
Halt all testing if memory array has too many failed addresses to be repaired
320
In accordance with the test pattern, select next address to be tested in memory array and return to step 306
322
End

Fig. 3

400



Field:	Data contents:
A	Header
B	Failed Address Length
C	Failed Address
D	Failed Data Length
E	Data Written
F	Data Read-Out
G	Failed Bit Locations

Fig. 4

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